Artix-7 FPGA AC701 Evaluation Kit (Vivado Design Suite 2013.3)

Getting Started Guide

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/10/2013	1.0	Initial Xilinx release.
04/17/2013	2.0	Updated for Vivado® Design Suite 2013.1. Updated Introduction, Basic Hardware Bring-up with Built-In Self-Test, AMS Bring-up with the AMS101 Evaluation Card, and Advanced Bring-up with Base Targeted Reference Design sections. Updated Figure 2.
07/10/2013	3.0	Updated for Vivado® Design Suite 2013.2.
11/19/2013	4.0	Updated version references for Vivado Design Suite from 2013.2 to 2013.3. Corrected the LED Status descriptions on page 24. Changed *Note* to *Caution* and strengthened the description in the power connection note on page 24. Revised all links and references in Appendix A, Additional Resources and revised links to web pages and documents throughout document to conform to latest style convention. Updated Figure 21, page 28 and Figure 22, page 28.
03/05/2014	4.0.1	Tech pubs update. Technical content not affected.

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Getting Started with the Artix-7 FPGA AC701 Evaluation Kit

Introduction

The Artix®-7 FPGA AC701 Evaluation Kit (Figure 1) provides a comprehensive, high-performance development and demonstration platform based on the XC7A200T FPGA for high-bandwidth and high-performance applications in multiple market segments. The built-in self-test (BIST), the AMS 101 evaluation card usage, and the Artix-7 FPGA Base Targeted Reference Design (TRD) are featured in this getting started guide.

Figure 1: **AC701 Evaluation Kit**

This Getting Started Guide is divided into two sections:

- Basic Hardware Bring-up: Enables hands-on operation of all the features in the BIST as well as evaluation of Analog Mixed Signal (AMS) using the AMS101 evaluation card.
- Advanced Bring-up: Enables hands-on operation with the base TRD, which features PCIe®, DDR3 memory, AXI stream interconnect, and AXI virtual FIFO controller IP cores—all supported through a custom evaluation graphical user interface (GUI).

AC701 Evaluation Kit Contents

- AC701 evaluation board featuring the XC7A200T FPGA
- Targeted reference design featuring DDR3, PCIe, and DMA
  - Including a full license for the Northwest Logic DMA
- AMS101 evaluation board
- Full seat Vivado® Design Suite: Design Edition
  - Node-locked, device-locked to the Artix-7 XC7A200T FPGA
- Additional downloadable content, including:
  - Reference designs, design examples, and demos
  - Board design files
  - Documentation
    - Hardware User Guide
    - Getting Started Guide
    - Reference Design User Guide
- 12V AC-adapter power supply
- Cables
  - RJ45 Ethernet cable
  - HDMI cable
  - Type-A to micro-B USB cable used for JTAG programming
  - Type-A to mini-B USB cable used for UART communication with board
- Software and reference designs, demos, and documents to quickly get started
- The AC701 BIST Design Files (RDF0220) are available from the AC701 Evaluation Kit Documentation webpage.

All user guides, board files, tutorials, example designs, and targeted reference designs are available from the AC701 Evaluation Kit Documentation webpage.

The tutorials and reference designs are useful for exploring the capabilities of the AC701 board and the Artix-7 FPGA. For additional information, see the Artix-7 Family FPGAs Product Table.

Basic Hardware Bring-up with Built-In Self-Test

Introduction

The BIST reference design tests many of the features of the Artix-7 FPGA AC701 Evaluation Kit and can be programmed into the FPGA via the JTAG interface.

Figure 2 and Table 1 provide an overview of the board features utilized by the BIST and the AMS101 evaluation card.

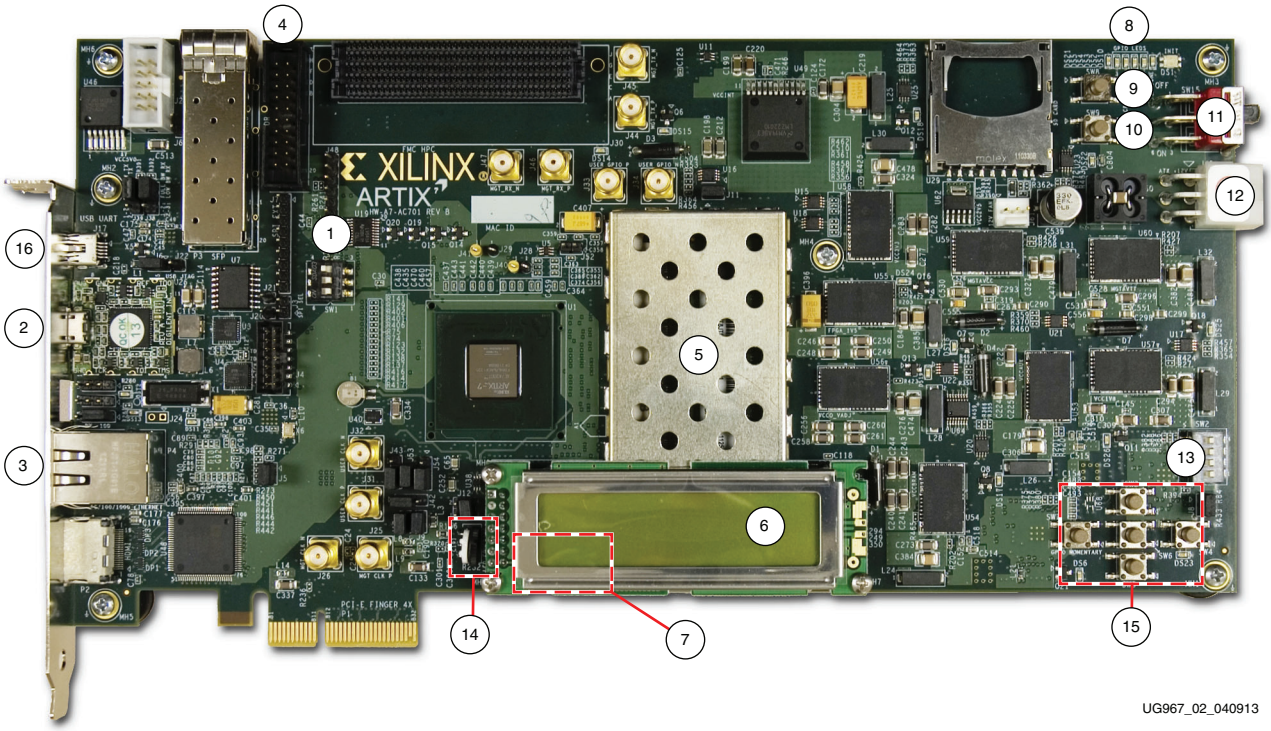


Figure 2: **AC701 Board Detail**

Table 1: **AC701 Board Features**

Callout	Component Description
1	SW1 Configuration Mode DIP Switch
2	Digilent JTAG connector
3	RJ45 Ethernet connector
4	XADC header
5	DDR3 external memory
6	LCD display
7	Rotary switch (under LCD)
8	Status LEDs and user LEDs
9	CPU reset button
10	Prog button
11	Power slide switch
12	12V power connector
13	User DIP switch
14	Contrast wheel
15	User push buttons
16	USB-UART connector

For a description of all features on the AC701 Board, see *AC701 Evaluation Board for the Artix-7 FPGA User* Guide (UG952) [Ref 1].

Test Setup Requirements

Note: This example design uses a Windows 7 PC flow and TeraTerm Pro.

The prerequisites for testing the design in hardware are:

- AC701 evaluation board with XC7A200T FPGA
- Type-A to mini-B USB cable (for UART)
- Type-A to micro-B USB cable (for JTAG)
- AC Power Adapter (12 VDC)
- TeraTerm Pro or other terminal program
- USB-UART drivers from Silicon Labs
- Vivado Design Suite installed on host PC

Hardware Test Board Setup

This section details the hardware setup and use of the terminal program for running the BIST application. It details step-by-step instructions for board bring-up. For more information on installing the tools and drivers, see the Boards and Kits Install Guide.

AC701 Evaluation Board Setup

1. Set DIP switch SW1 as shown in Figure 3 (ON, OFF, ON = `101`).

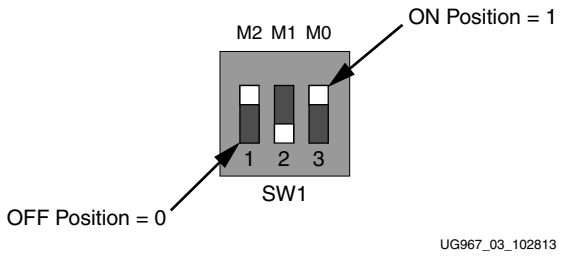


Figure 3: **SW1 Switch Settings for JTAG Programming Mode**

Hardware Bring-up

1. Place the AC701 board power switch SW12 to OFF.
2. Connect the AC701 board as shown in Figure 4.
3. Place the AC701 board power switch SW12 to ON.

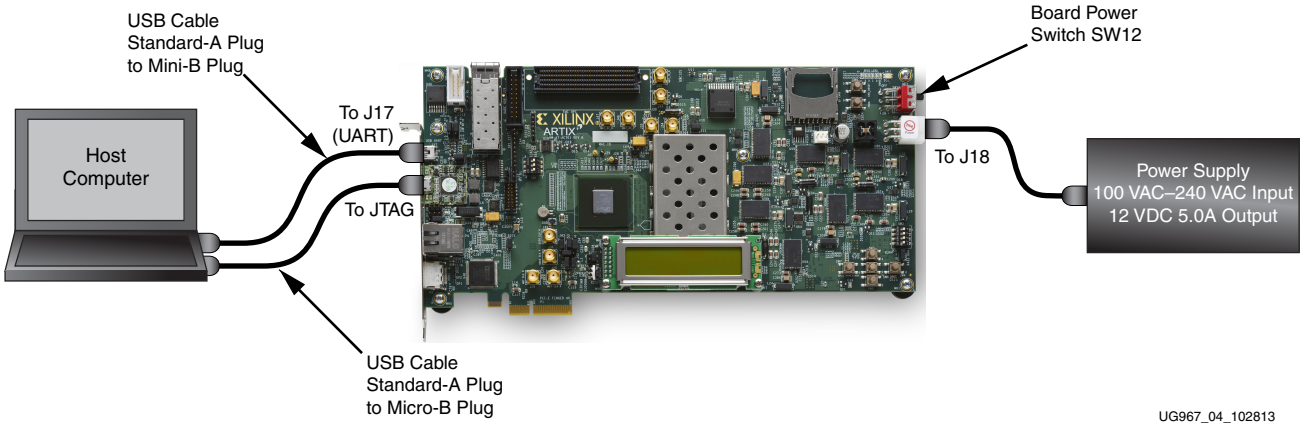


Figure 4: **AC701 Board with UART and 12V Adapter Cables Attached**

Install the Silicon Labs UART Device Driver.

1. Run the downloaded executable UART-USB driver file, listed in Test Setup Requirements (see Figure 5). This enables UART-USB communications with a host PC.

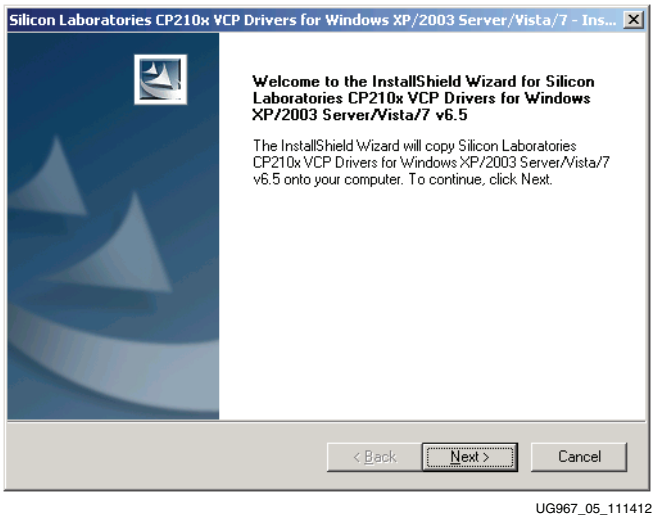
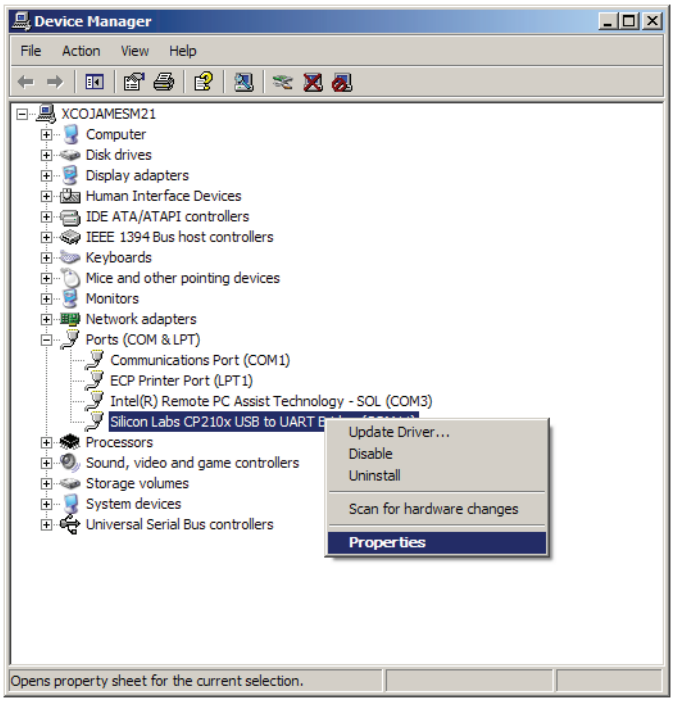

Silicon Laboratories CP210x VCP Drivers for Windows XP/2003 Server/Vista/7 - Ins...
Welcome to the InstallShield Wizard for Silicon Laboratories CP210x VCP Drivers for Windows XP/2003 Server/Vista/7 v6.5
The InstallShield Wizard will copy Silicon Laboratories CP210x VCP Drivers for Windows XP/2003 Server/Vista/7 v6.5 onto your computer. To continue, click Next.
< Back
Next >
Cancel
UG967_05_111412

Figure 5: **UART Cable Driver Installation Dialog**

2. Set the USB-UART connection to a known PORT in the Device Manager:
   a. Right-click the **Computer** desktop icon and select **Properties**.
   b. Click **Device Manager**.
   c. Right-click the Cypress device in the list, and select **Properties** (see Figure 6).



UG967_06_111412

Figure 6: **Selecting the Cypress Driver in the Device Manager**

d. Click the **Port Settings** tab, then click the **Advanced...** button.

e. Select an open COM port between COM1 and COM4 (see Figure 7).

Note: Steps and diagrams refer to a Windows host PC.

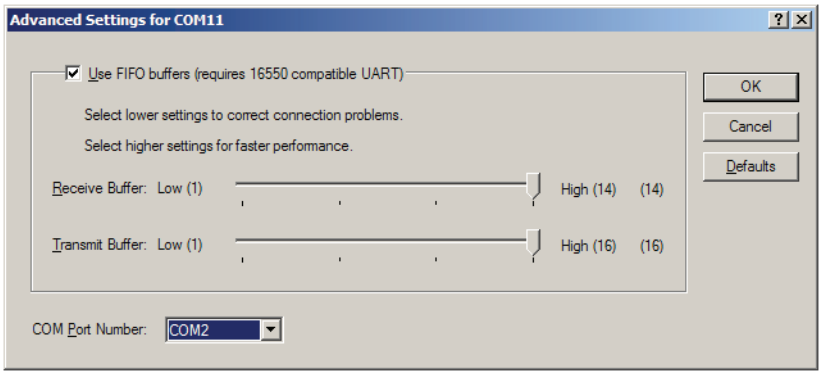

Advanced Settings for COM11
Use FIFO buffers (requires 16550 compatible UART)
Select lower settings to correct connection problems.
Select higher settings for faster performance.
Receive Buffer: Low (1) High (14) (14)
Transmit Buffer: Low (1) High (16) (16)
OK
Cancel
Defaults
COM Port Number: COM2

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Figure 7: **Setting the Port for the Cypress Driver**

Run the BIST Application

1. Download the AC701 BIST Design Files (RDF0220) from the AC701 Evaluation Kit Documentation webpage under the Example Designs section.
2. Unzip the design files to the `C:\` directory.
3. Start the installed terminal program.

4. Select **Setup > Serial Port…** and ensure that the settings match those shown in Figure 8:
   - **Baud rate**: 9600
   - **Data**: 8 bit
   - **Parity**: none
   - **Stop**: 1 bit
   - **Flow control**: none

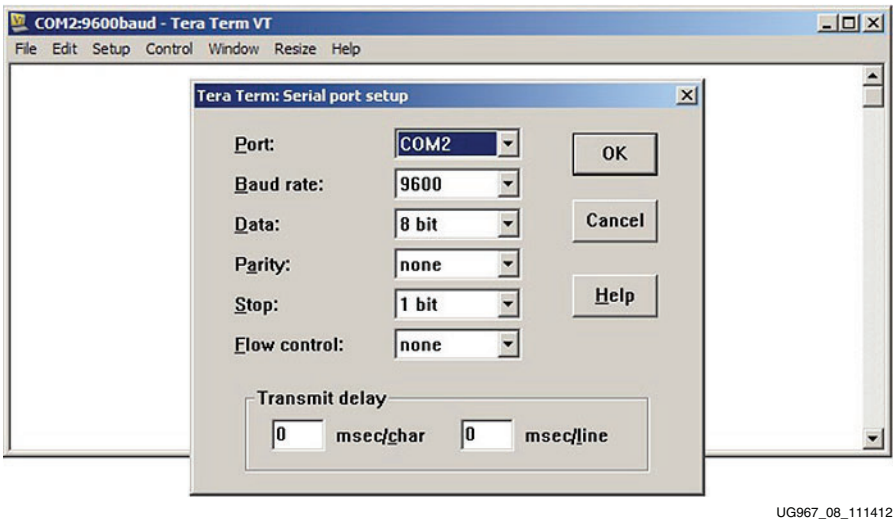

Figure 8: **Serial Port Setup**

5. In Vivado Design Suite, open a Tcl shell and type:

```
source C:/ac701_bist/ready_for_download/bist_download.tcl
```

6. Select the desired tests to run and observe the test results (see Figure 9).

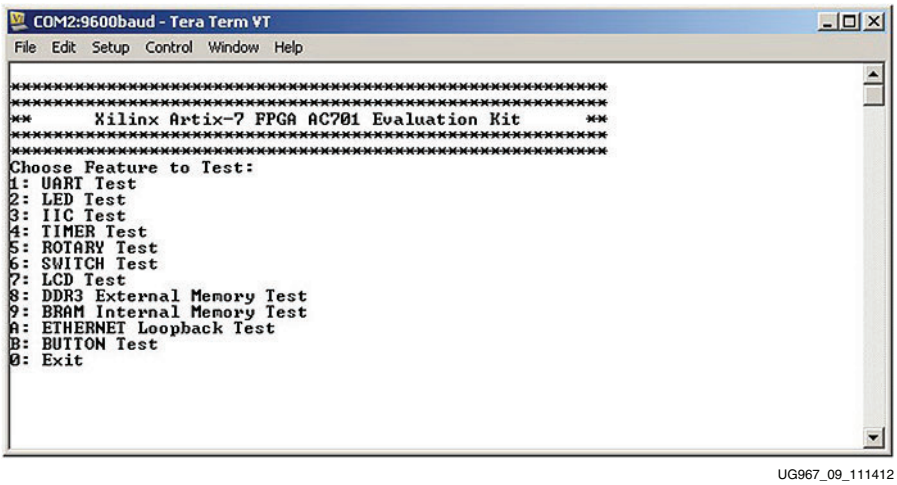

Figure 9: **BIST Main Menu**

AMS Bring-up with the AMS101 Evaluation Card

Introduction

The Artix-7 XC7A200T FPGA features two 1 Mega-samples per second (MSPS), 12-bit, Analog-to-Digital Converters (ADCs) built into the device for a range of applications including simple analog monitoring to more signal processing-intensive tasks such as linearization, calibration, oversampling, and filtering. The AC701 Evaluation Kit includes the hardware and software to evaluate the ADC feature. The AC701 Evaluation Kit also includes voltage, current and power monitoring for nine of the analog power supplies on the board. For evaluation of Xilinx Analog Mixed Signal (AMS) capability, these items in the kit are needed:

- Access to the AC701 board XADC header (see Figure 2)
- AMS101 evaluation card (see Figure 10 and Table 1)
- FPGA design files and software files
- *7 Series FPGA AMS Targeted Reference Design User Guide* (UG960) [Ref 1]
- USB-UART drivers from Silicon Labs

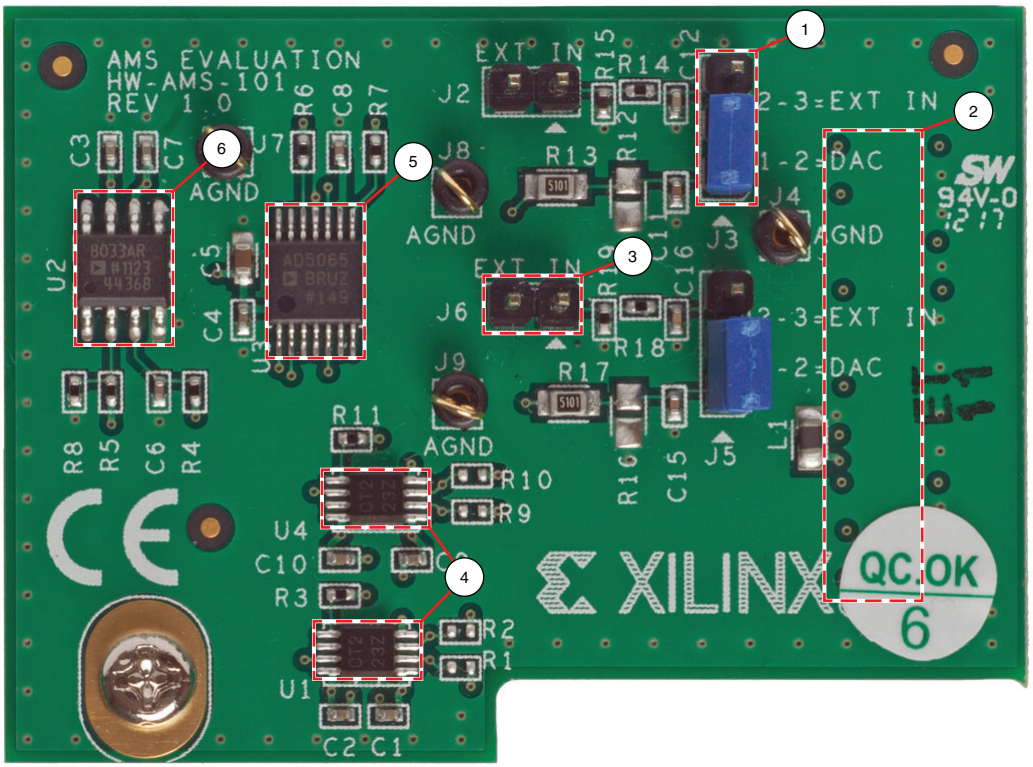

Figure 10: **AMS101 Evaluation Card**

Table 2: **AMS101 Evaluation Card Features**

Callout	Component Description
1	Jumpers to select DAC or external signal source.
2	20-pin connector to the XADC header on the AC701 board.

Table 2: **AMS101 Evaluation Card Features *(Cont'd)***

Callout	Component Description
3	Pins for external analog input signals.
4	Digital I/O level translators.
5	16-bit DAC to set analog test voltage.
6	Reference buffer for DAC.

Getting Started

1. Verify the USB-UART Silicon Labs drivers are installed as described in Install the Silicon Labs UART Device Driver., page 11.
2. Install the National Instruments LabVIEW run-time engine on the host PC:
   a. Go to the AC701 Evaluation Kit Documentation webpage.
   b. Under the *Documentation* heading, click on the appropriate Vivado software version. This will expand a list of available document types.
   c. Click on **Targeted Reference Designs**. This will open a list of files and documents.
   d. Click on **7 Series FPGA and Zynq-7000 AP SoC AMS Evaluator Installer for AMS Targeted Reference Design** to download `ams101_gui_installer.zip`.
   e. Unzip the files to a temporary directory and double-click `setup.exe` to install the LabVIEW run-time engine and AMS Evaluator software.
   f. After installation is complete, restart the host PC.
3. Extract the AMS design files before Evaluating AMS:
   a. Go to the AC701 Evaluation Kit Documentation webpage.
   b. Under the *Documentation* heading, click on the appropriate Vivado software version. This will expand a list of available document types.
   c. Click on **Targeted Reference Designs**. This will open a list of files and documents.
   d. Click on **AMS Targeted Reference Design for Artix-7 FPGA AC701 Evaluation Kit (RDF0278)** to download `rdf0278-ams101-ac701-trd.zip`.
   e. Unzip the files to a working directory on the host computer.

Evaluating AMS

1. Power off the AC701 board, connect the AMS101 card, and re-apply power to the hardware.
   a. Connect the AMS101 evaluation card to the AC701 board, making sure the notch on the XADC header lines up correctly with the connector on the AMS101 evaluation card.
2. Implement the design to the Artix-7 XC7A200T-2 FB676 FPGA from the AC701 AMS design file `xadc_eval_design_ac701_v1_0` previously downloaded.
   a. Open Vivado Design Suite. Here is one example path:

      ```
      Start menu/Xilinx Design Tools/Vivado 2013.3
      ```

   b. Create a Vivado Project.

c. Open Hardware Session.

d. Open a new hardware target and run through the wizard.

e. Click the **open_cable** command and select **OK**.

f. Open `xadc_eval_design.bit` from the AC701 board AMS design folder:
xadc_eval_design_ac701_v1_0 > ready_to_test > xadc_eval_design.bit

3. Open the AMS Evaluator tool.

a. Running the setup program loads the AMS101 Evaluator GUI with the Xilinx logo on your desktop. Figure 11 shows the AMS101 Evaluator after opening. From here, click the **Connect** button. When the button is green, click the **Collect Data** button in the center to quickly evaluate the analog signals in the time and frequency domain, display linearity, verify the **XADC Registers** settings, and measure the internal temperature sensor and supply voltages.

b. **Collect Data** button in the center to quickly evaluate the analog signals in the time and frequency domain, display linearity, verify the XADC register settings, and measure the internal temperature sensor and supply voltages.

c. Figure 12 shows the XADC results in the frequency domain.

d. The AMS101 evaluation card provides a dual 16-bit DAC for use as an analog test source. External analog signals can also be applied to the card. For a more extensive explanation of the AMS101 evaluation card and the various functions in the AMS Evaluator tool, see *AMS101 Evaluation Card User Guide* (UG886) [Ref 16].

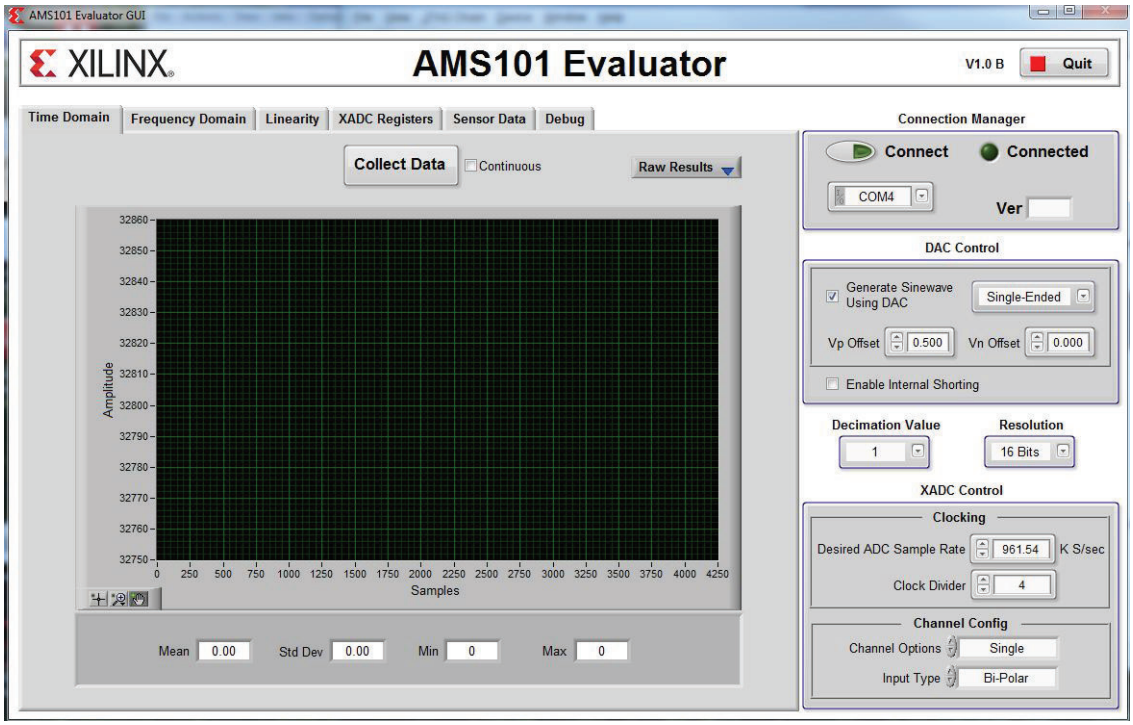

Figure 11: **AMS Evaluator Tool**

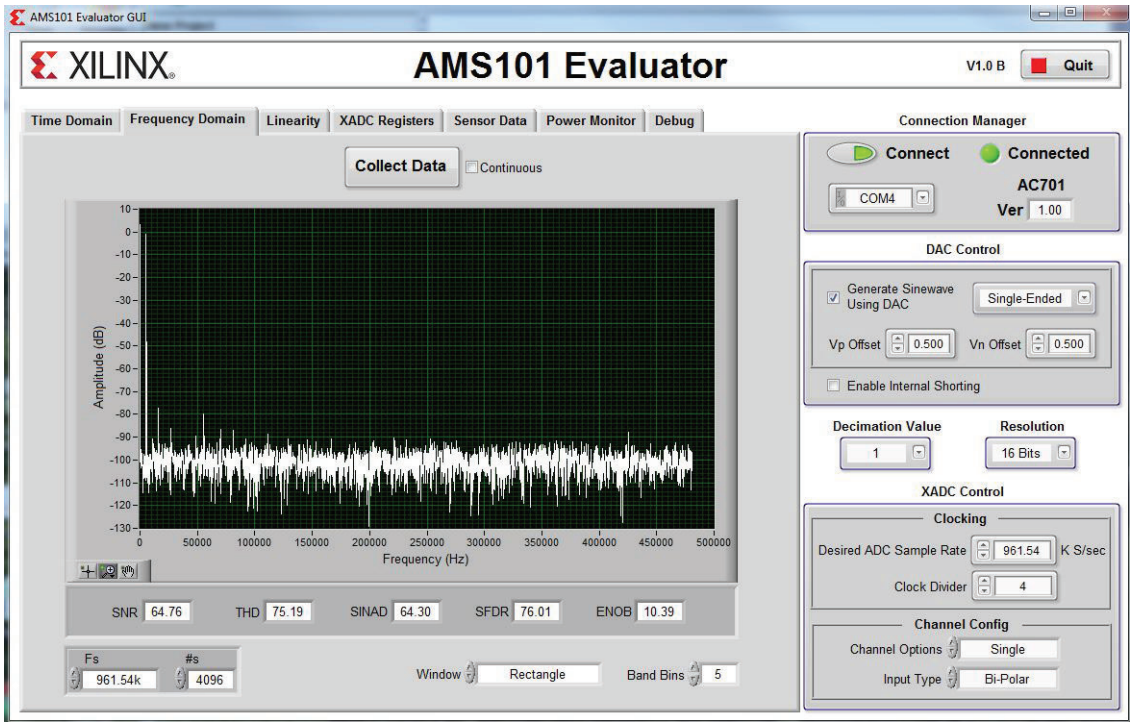

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Figure 12: **XADC Fast Fourier Transform Result**

Power Monitoring

In addition to measuring the analog signals from the AMS101 evaluation card, the AC701 also uses the XADC as a system monitoring solution for measuring the voltage, load current and calculated power for nine of the AC701 board analog power supplies. By offering 12-bits, 1 MSPS and up to 17 externally multiplexed inputs, the XADC is a good solution for monitoring voltage and current on all Artix-7 FPGA applications. Figure 13 shows an example of the AC701 monitoring V_{CCINT}, V_{CCAUX}, V_{CCBRAM} and the 1.5V supply.

In conjunction with the AMS Evaluator, the AC701 AMS reference design also measures the voltages, current and power for V_{CCO_ADJ}, the 1.8V supply, the 3.3V supply, MGTAVCC and MGTAVTT.

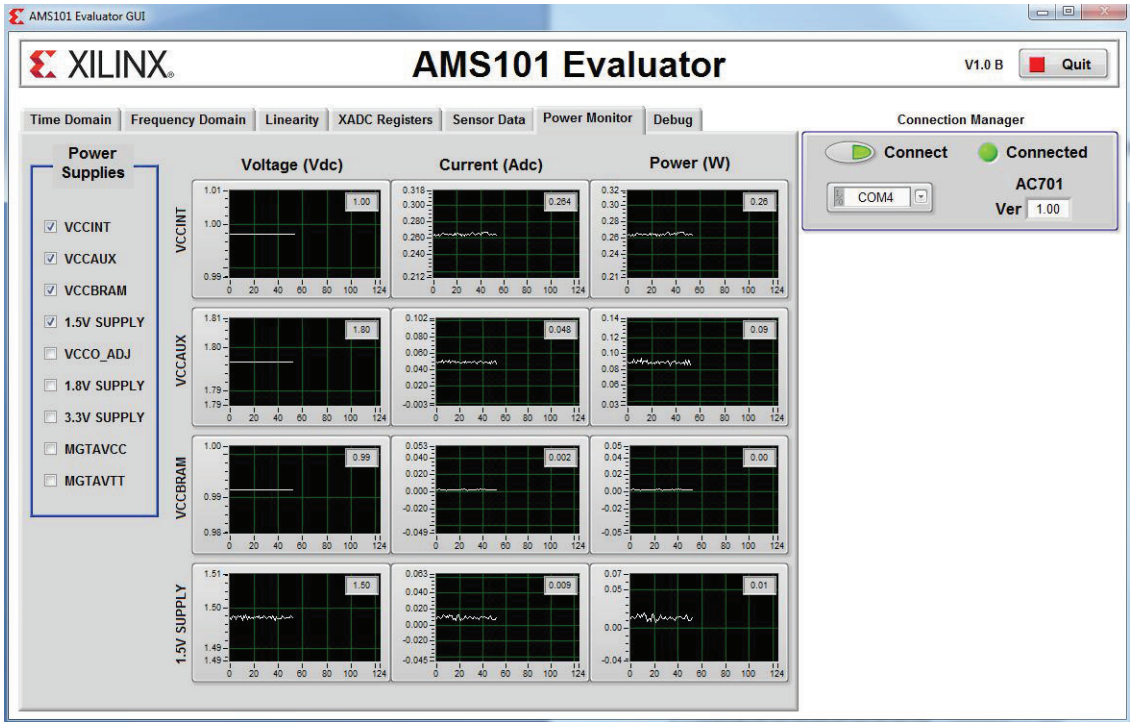

Figure 13: **Voltage, Current and Power Monitoring on AC701 Board Supplies**

Advanced Bring-up with Base Targeted Reference Design

Introduction

Figure 14 depicts the block-level overview of the Artix-7 FPGA base Targeted Reference Design (TRD) which delivers up to 10 Gb/s of performance per direction.

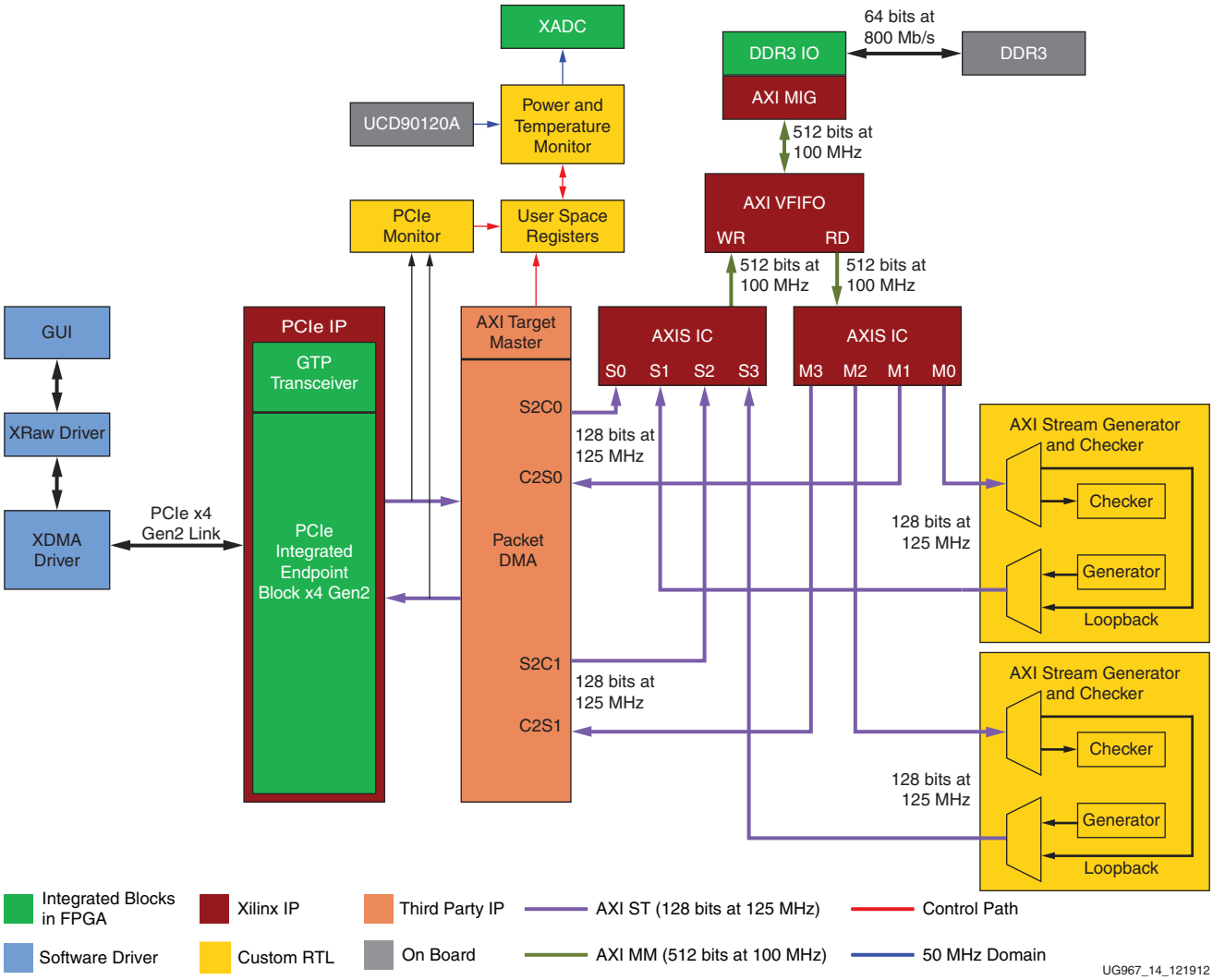

Figure 14: **Artix-7 FPGA Base TRD Block Diagram**

The intent of this design is to demonstrate a high performance data transfer system using the PCI Express® x4 GEN2 endpoint with a high performance scatter-gather packet DMA controller from NorthWest Logic and DDR3 64-bit SODIMM memory operating at 800 Mb/s.

The PCIe® endpoint and DMA controller together are responsible for the movement of data between a PC and an FPGA. S2C implies data movement from a PC to an FPGA and C2S implies data movement from an FPGA to a PC. A DDR3 SDRAM (64-bit, 800 Mb/s or 400 MHz) is used for packet buffering — a virtual FIFO layer facilitates the use of DDR3

memory as multiple FIFOs. Additionally, the design provides power monitoring capability based on a PicoBlaze™ embedded processor.

For software, the design provides 32-bit Linux drivers targeting the Fedora 16 platform and a graphical user interface (GUI) which controls the tests and monitors the status.

Features

Base Features

This section lists the features of the Targeted Reference Design.

- PCI Express v2.1 compliant x4 endpoint operating at 5Gb/s/lane/direction
  - PCIe transaction interface utilization monitor
  - MSI & Legacy interrupt support
- Bus Mastering Scatter-gather DMA
  - Multichannel DMA
  - AXI4-Stream interface for data
  - AXI4 interface for register space access
  - DMA performance monitor
  - Full duplex operation
    - Independent transmit and receive channels
- Virtual FIFO layer over DDR3 memory
  - Provides 4 channel design (4 FIFOs in DDR3 SODIMM)

Application Features

- PicoBlaze processor-based PVT Monitoring
  - Built-in hardware to monitor power by reading the TI UCD90120A power controller chip included on the AC701 evaluation board
  - Built-in hardware to monitor die temperature by way of a Xilinx Analog-to-Digital Converter

Test Setup Requirements

The prerequisites for testing the design in hardware are

- AC701 evaluation board with XC7A200T FPGA
- Design consisting of:
  - Design source files
  - Device driver files
  - FPGA programming files
  - Documentation
- Vivado Design Edition
- Type-A to micro-B USB cable
- Fedora 16 LiveDVD

- A PC with PCIe v2.1 compliant slot. For a complete list of recommended machines, and all known issues, see Artix-7 FPGA Base Targeted Reference Design Master Answer Record (AR 53372).

  Note: The PC could also have Fedora 16 Linux OS installed.

Hardware Demonstration Setup

This section details the hardware setup and use of the provided control and monitoring application and GUI to assist in getting started quickly with the hardware. Step-by-step explanations are provided on hardware bring-up, software bring-up, and the use of the application GUI.

Board Setup

This section details how to set up the AC701 evaluation board as required for demonstrating the TRD.

Setting the AC701 Jumpers And Switches

1. Turn off the power to the AC701 board and verify the switch and jumper settings are as shown in Table 3, Table 4, and Figure 15.

Table 3: **AC701 Board Required Jumper Settings**

Jumper	Function	Setting
J12	PCIe endpoint configuration width; 4-lane design	3-4

Table 4: **AC701 Board Required Switch Settings**

Switch	Function/Type		Setting
SW15	Board power slide-switch		off
SW2	User GPIO DIP switch		
	4		off
	3		off
	2		off
	1		off
SW1	Positions 1, 2, and 3 set configuration mode		
	3	001 – Master SPI 101 – JTAG	on
	2		off
	1		off

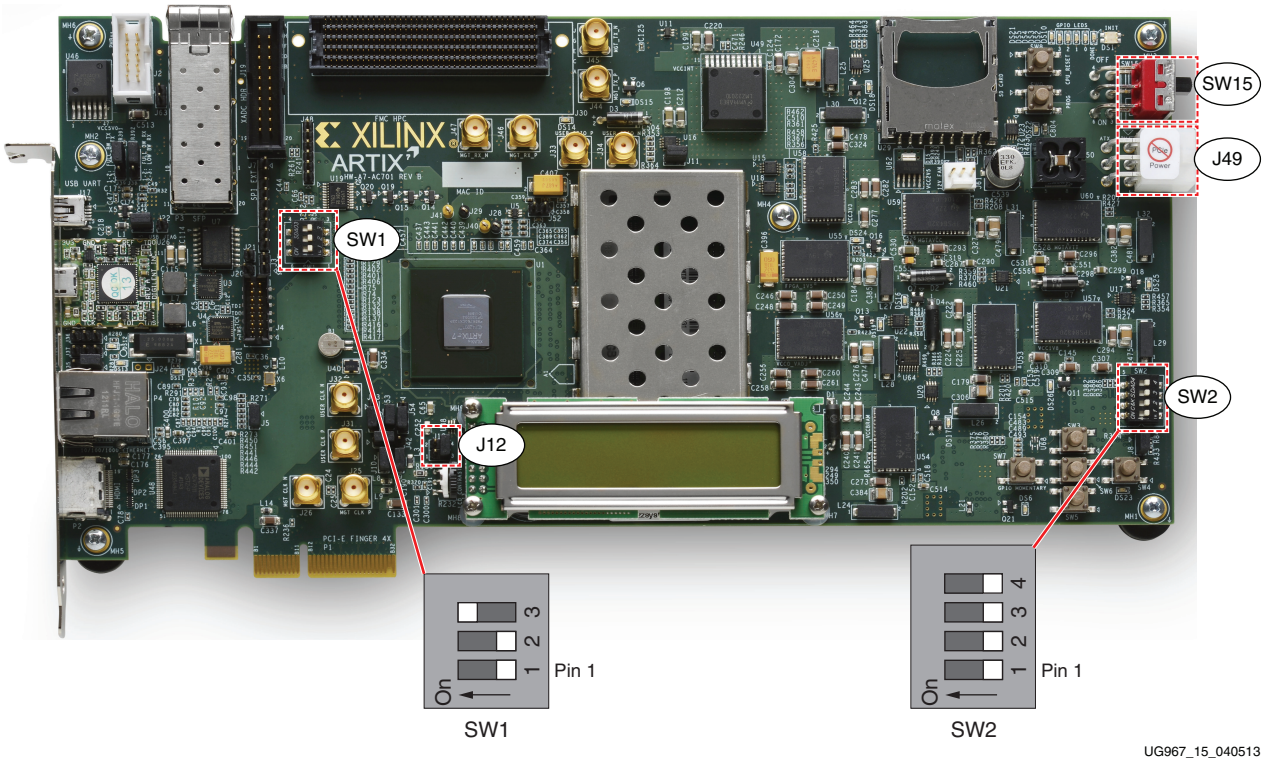

Figure 15: **AC701 Board Switch and Jumper Locations**

Hardware Bring Up

All procedures listed in the subsequent sections require super-user access on a Linux PC. When using the Fedora 16 LiveDVD provided with the kit, super-user access is granted by default due to the manner in which the kernel image is built. If not using the LiveDVD, it is important to ensure that super-user access is granted.

1. With the host PC powered off, insert the AC701 board into the selected PCIe x4 (or wider) edge connector (see Figure 16). The PCI Express specification allows for a smaller lane width endpoint to be installed into a larger lane width PCIe connector.

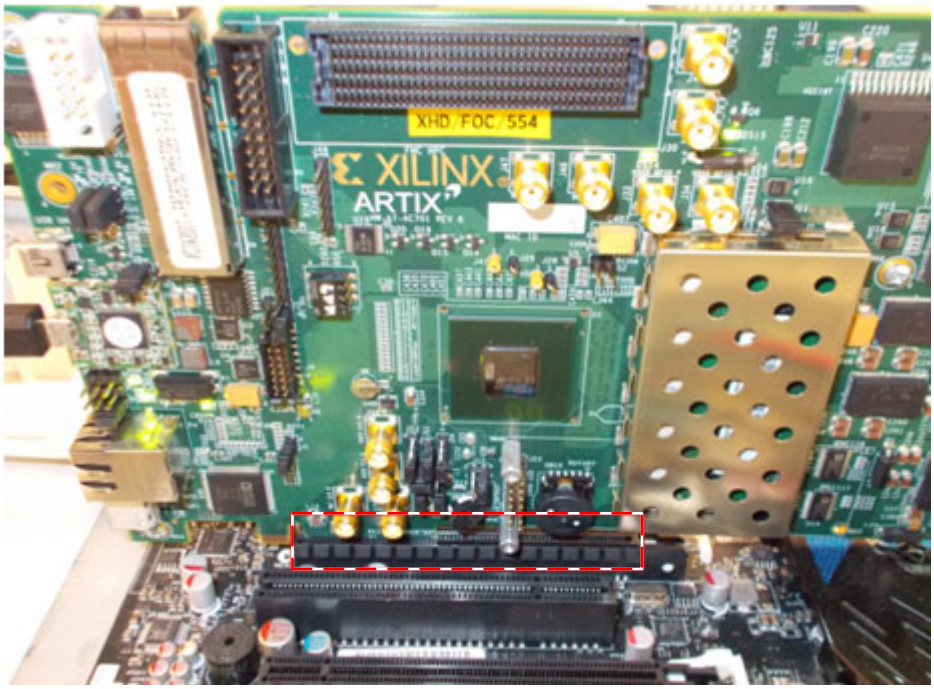

Figure 16: **AC701 Board Installed in a PCIe x16 Connector**

2. Connect the 12V ATX power supply 4-pin connector to the board as shown in Figure 17.

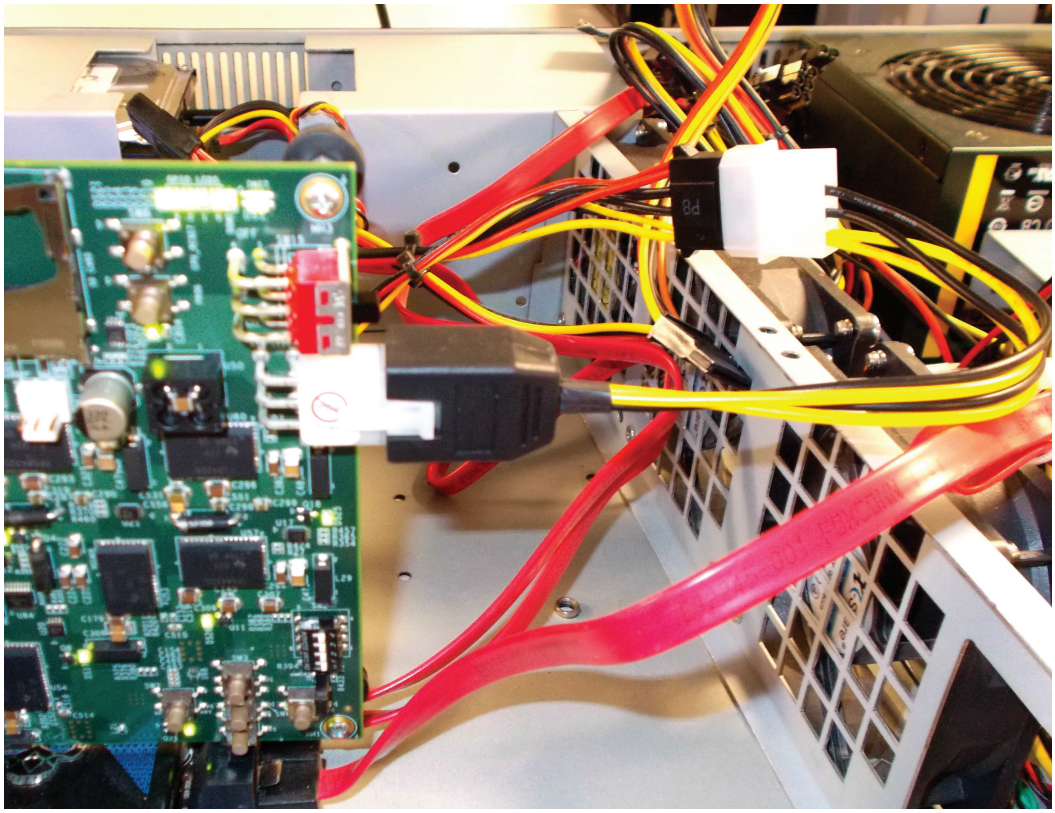

Figure 17: **Power Supply Connection**

Caution! Do NOT plug a PC ATX power supply 6-pin connector into J49 on the AC701 board The ATX 6-pin connector has a different pinout than J49. Connecting an ATX 6-pin connector into J49 will damage the AC701 board and void the board warranty.

3. To avoid loose contact issues, make sure the connections are secure. Turn ON the SW15 switch, apply power to the system, insert the Fedora LiveDVD, and change the boot order to boot from the DVD.
4. Check the status of the design using the AC701 board LEDs. The design provides status with the GPIO LEDs located on the upper right portion of the AC701 board. When the PC is powered on and the TRD has successfully configured, the LED status from left to right indicates:
   - **LED position 1**: ON if DDR3 is calibrated
   - **LED position 2**: ON if the lane width is x4, else flashing
   - **LED position 3**: Heart beat LED, flashes if PCIe user clock is present
   - **LED position 4**: ON if the PCIe link is up

Figure 18 shows the location of the status LEDs.

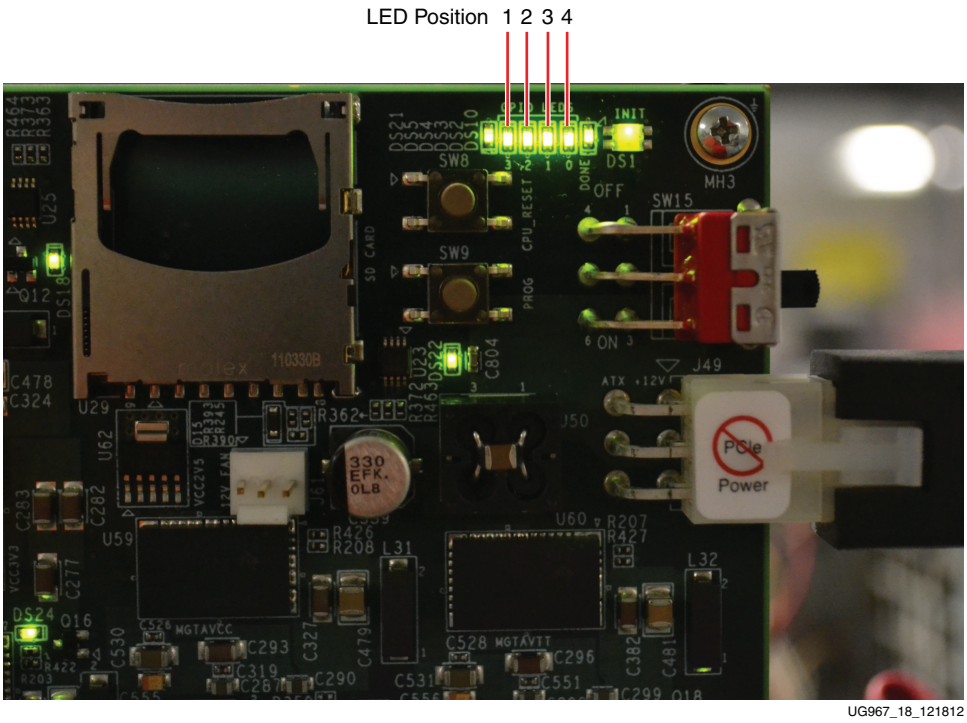

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Figure 18: **GPIO LEDs Indicating TRD Status**

Linux Driver Installation

The following sections describe installing the device drivers for the Artix-7 FPGA base TRD after completion of the prior steps.

1. If the Fedora 16 Linux OS is currently installed on the PC, boot as a root-privileged user and skip to step 4.
2. To boot from the Fedora 16 LiveDVD provided in the kit, place the DVD in the PC DVD-ROM drive. The Fedora 16 Live Media is for Intel-compatible PCs. The DVD contains a complete, bootable 32-bit Fedora 16 environment with the proper packages installed for the TRD demonstration environment. The PC boots from the DVD-ROM drive and logs into a liveuser account. This account has kernel development root privileges required to install and remove device driver modules.

   Note: It might be necessary to adjust the PC BIOS boot order settings to ensure that the DVD-ROM drive is the first drive in the boot order. Refer to the PC user manual for the proper procedure to set the BIOS boot order.

The PC should boot from the DVD-ROM drive. The images in Figure 19 are seen on the monitor during startup.

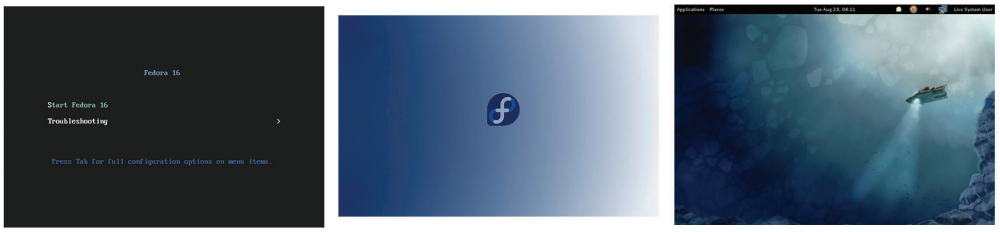

Figure 19: **Fedora 16 LiveDVD Boot Sequence**

3. After Fedora boots, open a terminal window (click **Activities > Application**, scroll down, and click the **Terminal** icon).

   To determine if the PCIe integrated block is detected, at the terminal command prompt, type:

   ```
   $ lspci
   ```

   The `lspci` command displays the PCI and PCI Express buses of the PC. On the bus corresponding to the PCIe connector holding the AC701 board, look for the message:

   ```
   Memory controller: Xilinx Corporation Device 7042
   ```

   This message confirms that the design programmed into the AC701 board is detected by the BIOS and the Fedora 16 OS. The bus number varies depending on the PC motherboard and slot used.

Figure 20 shows an example of the output from the `lspci` command. The highlighted region shows that Xilinx device 7042 has been located by the BIOS on bus number 3 (03:00.0 = bus:dev.function).

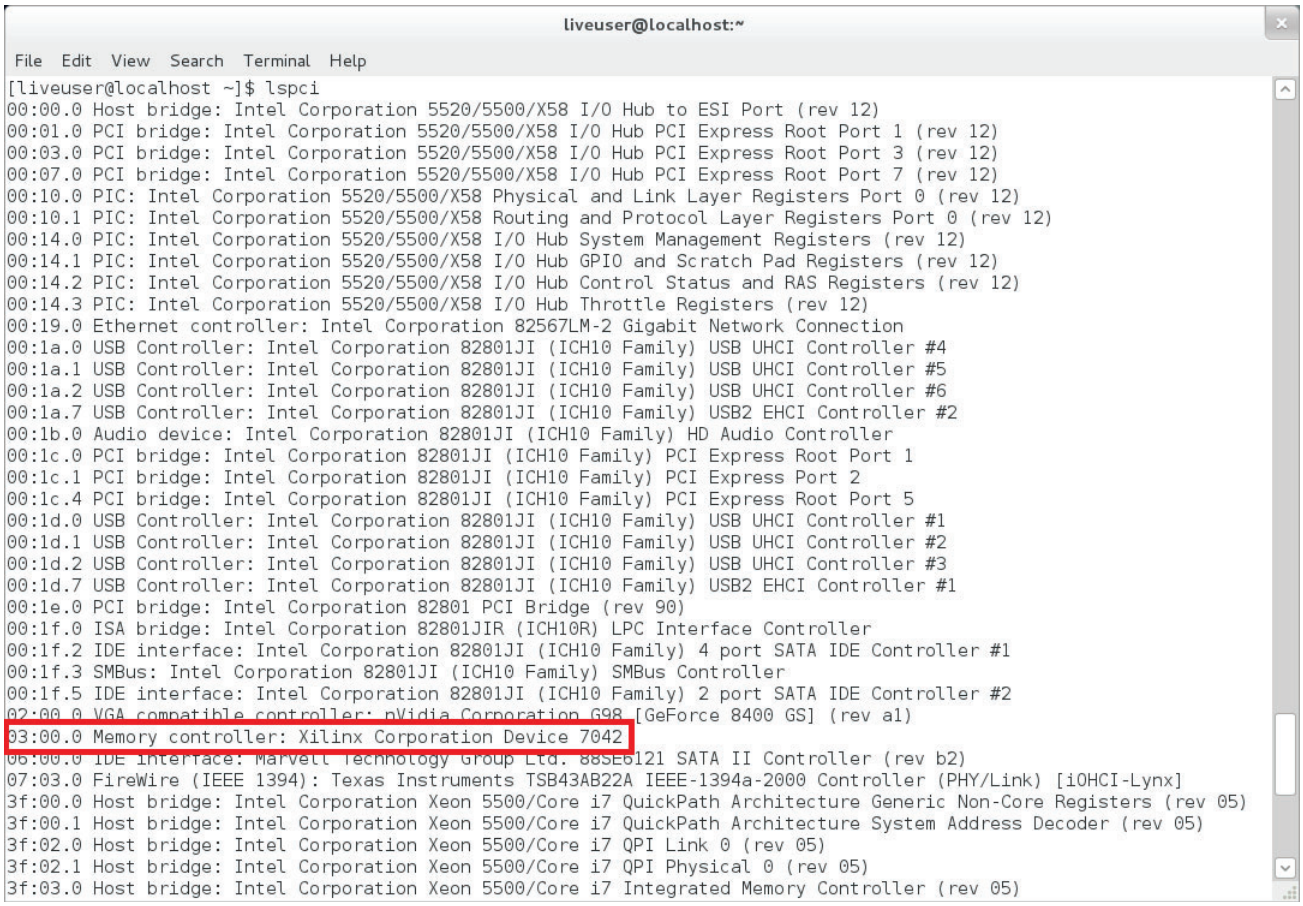
liveuser@localhost:~
File Edit View Search Terminal Help
[liveuser@localhost ~]$ lspci
00:00.0 Host bridge: Intel Corporation 5520/5500/X58 I/O Hub to ESI Port (rev 12)
00:01.0 PCI bridge: Intel Corporation 5520/5500/X58 I/O Hub PCI Express Root Port 1 (rev 12)
00:03.0 PCI bridge: Intel Corporation 5520/5500/X58 I/O Hub PCI Express Root Port 3 (rev 12)
00:07.0 PCI bridge: Intel Corporation 5520/5500/X58 I/O Hub PCI Express Root Port 7 (rev 12)
00:10.0 PIC: Intel Corporation 5520/5500/X58 Physical and Link Layer Registers Port 0 (rev 12)
00:10.1 PIC: Intel Corporation 5520/5500/X58 Routing and Protocol Layer Registers Port 0 (rev 12)
00:14.0 PIC: Intel Corporation 5520/5500/X58 I/O Hub System Management Registers (rev 12)
00:14.1 PIC: Intel Corporation 5520/5500/X58 I/O Hub GPIO and Scratch Pad Registers (rev 12)
00:14.2 PIC: Intel Corporation 5520/5500/X58 I/O Hub Control Status and RAS Registers (rev 12)
00:14.3 PIC: Intel Corporation 5520/5500/X58 I/O Hub Throttle Registers (rev 12)
00:19.0 Ethernet controller: Intel Corporation 82567LM-2 Gigabit Network Connection
00:1a.0 USB Controller: Intel Corporation 82801JI (ICH10 Family) USB UHCI Controller #4
00:1a.1 USB Controller: Intel Corporation 82801JI (ICH10 Family) USB UHCI Controller #5
00:1a.2 USB Controller: Intel Corporation 82801JI (ICH10 Family) USB UHCI Controller #6
00:1a.7 USB Controller: Intel Corporation 82801JI (ICH10 Family) USB2 EHCI Controller #2
00:1b.0 Audio device: Intel Corporation 82801JI (ICH10 Family) HD Audio Controller
00:1c.0 PCI bridge: Intel Corporation 82801JI (ICH10 Family) PCI Express Root Port 1
00:1c.1 PCI bridge: Intel Corporation 82801JI (ICH10 Family) PCI Express Port 2
00:1c.4 PCI bridge: Intel Corporation 82801JI (ICH10 Family) PCI Express Root Port 5
00:1d.0 USB Controller: Intel Corporation 82801JI (ICH10 Family) USB UHCI Controller #1
00:1d.1 USB Controller: Intel Corporation 82801JI (ICH10 Family) USB UHCI Controller #2
00:1d.2 USB Controller: Intel Corporation 82801JI (ICH10 Family) USB UHCI Controller #3
00:1d.7 USB Controller: Intel Corporation 82801JI (ICH10 Family) USB2 EHCI Controller #1
00:1e.0 PCI bridge: Intel Corporation 82801 PCI Bridge (rev 90)
00:1f.0 ISA bridge: Intel Corporation 82801JIR (ICH10R) LPC Interface Controller
00:1f.2 IDE interface: Intel Corporation 82801JI (ICH10 Family) 4 port SATA IDE Controller #1
00:1f.3 SMBus: Intel Corporation 82801JI (ICH10 Family) SMBus Controller
00:1f.5 IDE interface: Intel Corporation 82801JI (ICH10 Family) 2 port SATA IDE Controller #2
02:00.0 VGA compatible controller: nVidia Corporation G98 [GeForce 8400 GS] (rev a1)
03:00.0 Memory controller: Xilinx Corporation Device 7042
06:00.0 IDE interface: Marvell Technology Group Ltd. 88SE6121 SATA II Controller (rev b2)
07:03.0 FireWire (IEEE 1394): Texas Instruments TSB43AB22A IEEE-1394a-2000 Controller (PHY/Link) [iOHCI-Lynx]
3f:00.0 Host bridge: Intel Corporation Xeon 5500/Core i7 QuickPath Architecture Generic Non-Core Registers (rev 05)
3f:00.1 Host bridge: Intel Corporation Xeon 5500/Core i7 QuickPath Architecture System Address Decoder (rev 05)
3f:02.0 Host bridge: Intel Corporation Xeon 5500/Core i7 QPI Link 0 (rev 05)
3f:02.1 Host bridge: Intel Corporation Xeon 5500/Core i7 QPI Physical 0 (rev 05)
3f:03.0 Host bridge: Intel Corporation Xeon 5500/Core i7 Integrated Memory Controller (rev 05)

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Figure 20: **PCI and PCI Express Bus Devices**

4. Go to the AC701 Evaluation Kit Documentation webpage.
   a. Under Documentation, click **2013.3** to expand the list of 2013.3 documentation.
   b. Under By Document Type, click **Targeted Reference Designs** to open a window listing design files and documents.
   c. Click on the RDF0278 link and save the file `a7_base_trd` folder to the desktop (or a folder of choice).

   Note: This operation requires root privileges.

   Double-click the copied `a7_base_trd` folder.

The screen capture in Figure 21 shows the content of the `a7_base_trd` folder.

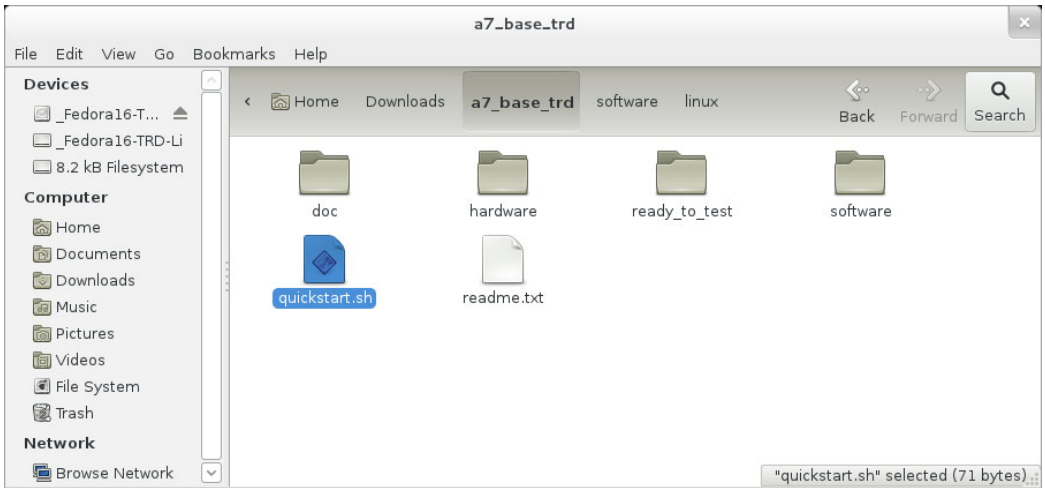

Figure 21: **Structure of a7_base_trd Directory**

5. Right-click on the script (`quickstart.sh`), select **Properties**. In the Permission tab, check the **Allow executing file as program** box. The script is now executable. To run the script, double-click `quickstart.sh` and select **Run in Terminal**.

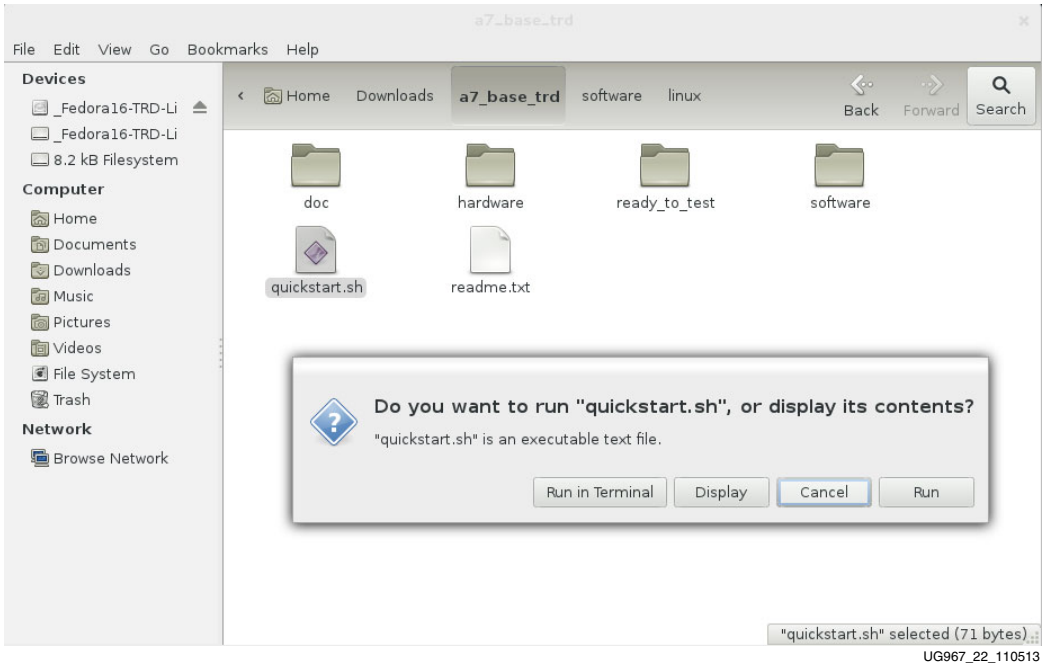

Figure 22: **Running the quickstart.sh Script**

6. The GUI showing driver installation options appears as shown in Figure 23. Subsequent steps demonstrate the GUI operation by installing and removing drivers. Click **Install**.

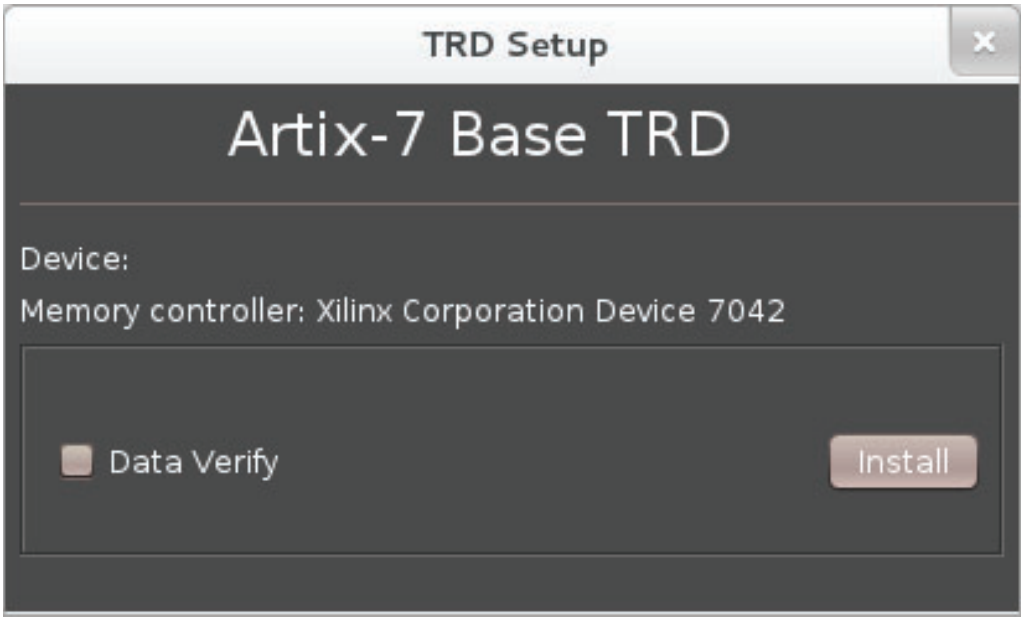

Figure 23: **Artix-7 FPGA Base TRD Driver Installation GUI**

After installing the driver, the control and monitoring user interface appears as shown in Figure 24. The control view shows control parameters such as test mode (loopback, generator, or checker) and packet length. The system monitor tab shows system power and temperature. The GUI also provides an LED indicator for DDR3 memory calibration.

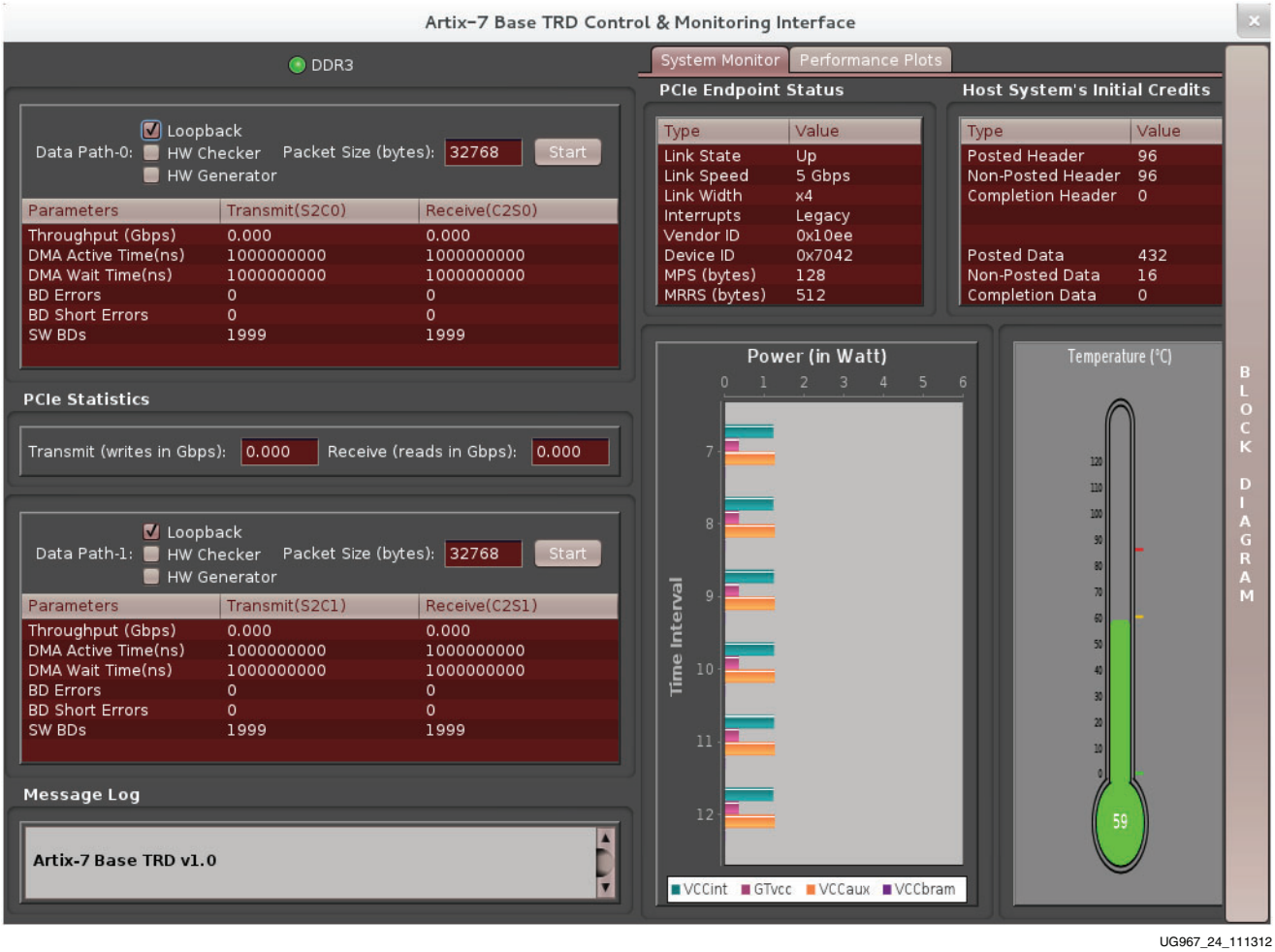

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Figure 24: **Artix-7 FPGA Base TRD Control and Monitoring Interface**

Using the Application GUI

The transmission and reception of data is configured through the application GUI. The GUI displays collected statistics and other status information.

At startup, the GUI displays a launching page that detects the PCIe device for this design (Vendor ID = 0x10EE and Device ID = 0x7042). When the appropriate device is detected, driver installation is allowed to proceed. An additional option is available which allows the enabling of a data integrity check. Upon successful installation of the drivers, the control and monitoring interface appears.

GUI Control Function

These parameters are controlled with the GUI:

- Packet size for traffic generation.

- Test selection:
  - Loopback
  - HW checker
  - HW Generator

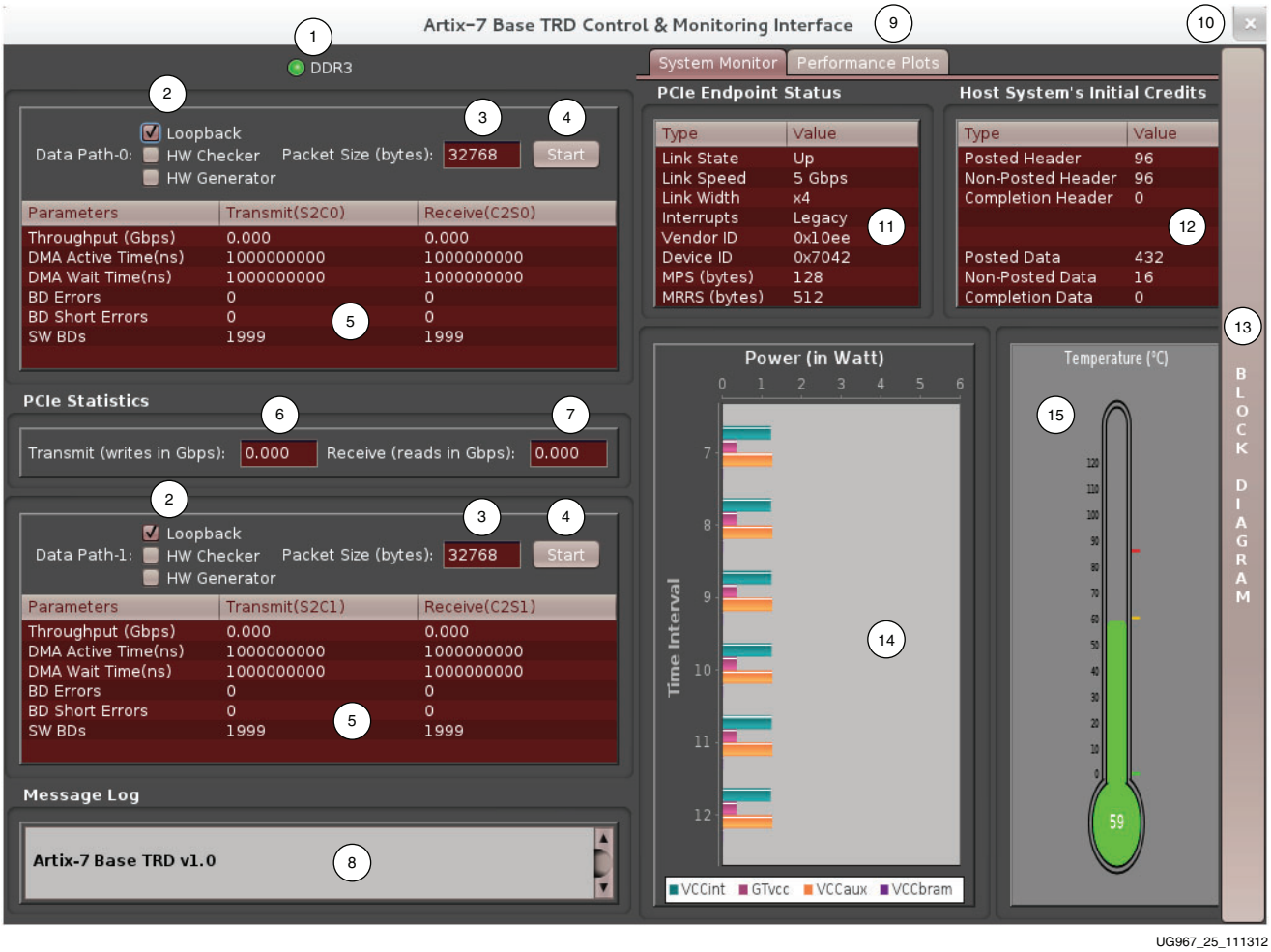
GUI Monitor Function

The driver always maintains information about the hardware status. The GUI periodically issues an I/O Control, `ioctl()`, to read the status information which is comprised of:

- PCIe link and device status
- DMA controller status
- Power status

The driver maintains a set of circular arrays to hold second-by-second sampling points of various statistics which are periodically collected by the performance monitor handler.

The various GUI indicators and controls are detailed in Figure 25 and Table 5.



UG967_25_111312

Figure 25: **Control and Monitoring Interface**

Table 5: **Control and Monitoring Interface Components**

Callout	Component	Component Description
1	Led Indicator	Indicates DDR3 calibration information; Green on calibration, red otherwise
2	Test Option	Options to select Loopback, HW Generator, or HW checker
3	Packet size	Packet size for the test run with allowed packet size shown as a tool tip
4	Test start/stop control	Button to control the start and end of the test
5	DMA statistics	• **Throughput (Gb/s)**: DMA payload throughput in gigabits per second for transmit and receive controllers • **DMA Active Time (ns)**: The time in nanoseconds that the DMA controller has been active in the last second • **DMA Wait Time (ns)**: The time in nanosecond that the DMA controller waited for the software to provide more descriptors • **BD Errors**: Indicates a count of buffer descriptors (BD) that caused a DMA error as indicated by the error status field in the descriptor update • **BD Short Errors**: Indicates a short error in the buffer descriptors in the transmit direction when the entire buffer specified by length in the descriptor could not be fetched (Not applicable to the receive direction) • **SW BDs**: Indicates the total count of buffer descriptors set up in the descriptor ring
6	PCIe Transmit (writes in Gb/s)	Reports transmitted (endpoint card to host) throughput as obtained from the PCIe endpoint hardware performance monitor
7	PCIe Receive (reads in Gb/s)	Reports received (host to endpoint card) throughput as obtained from the PCIe endpoint hardware performance monitor
8	Message log	Text box showing informational messages, warnings, or errors
9	Performance plots	Click this tab to plot the PCIe transactions on the AXI4-Stream interface and show the payload statistics graph based on the DMA controller performance monitor
10	Close button	Click this button to close the GUI
11	PCIe Endpoint Status	Reports the contents of various PCIe endpoint configuration fields as reported in the endpoint configuration space
12	Host System's Initial Credits	Initial flow control credits advertised by the host system after link training with the endpoint (A value of zero implies infinite flow control credits)
13	Block diagram button	Click this button to show a case block diagram of each mode currently running
14	Power statistics	Power in Watt plotted for the VCCINT, GTVCC, VCCAUX, and VCCBRAM rails
15	Temperature	Monitors the current die temperature

Notes:

1. Items 2 through 5 are duplicated for each of the two datapaths.

The GUI was developed using the JAVA environment. The Java Native Interface (JNI) was used to build the bridge between the driver and the GUI. This code can also be used with the Windows operating system with only minor changes.

Evaluating the TRD

1. To start the data traffic on the two datapaths:
   a. Click **Start** on Datapath-0 as shown in Figure 26. This enables the driver to start generating the data for Datapath-0.
   b. Click **Start** on Datapath-1 as shown in Figure 26. This enables the driver to start generating the data for Datapath-1.

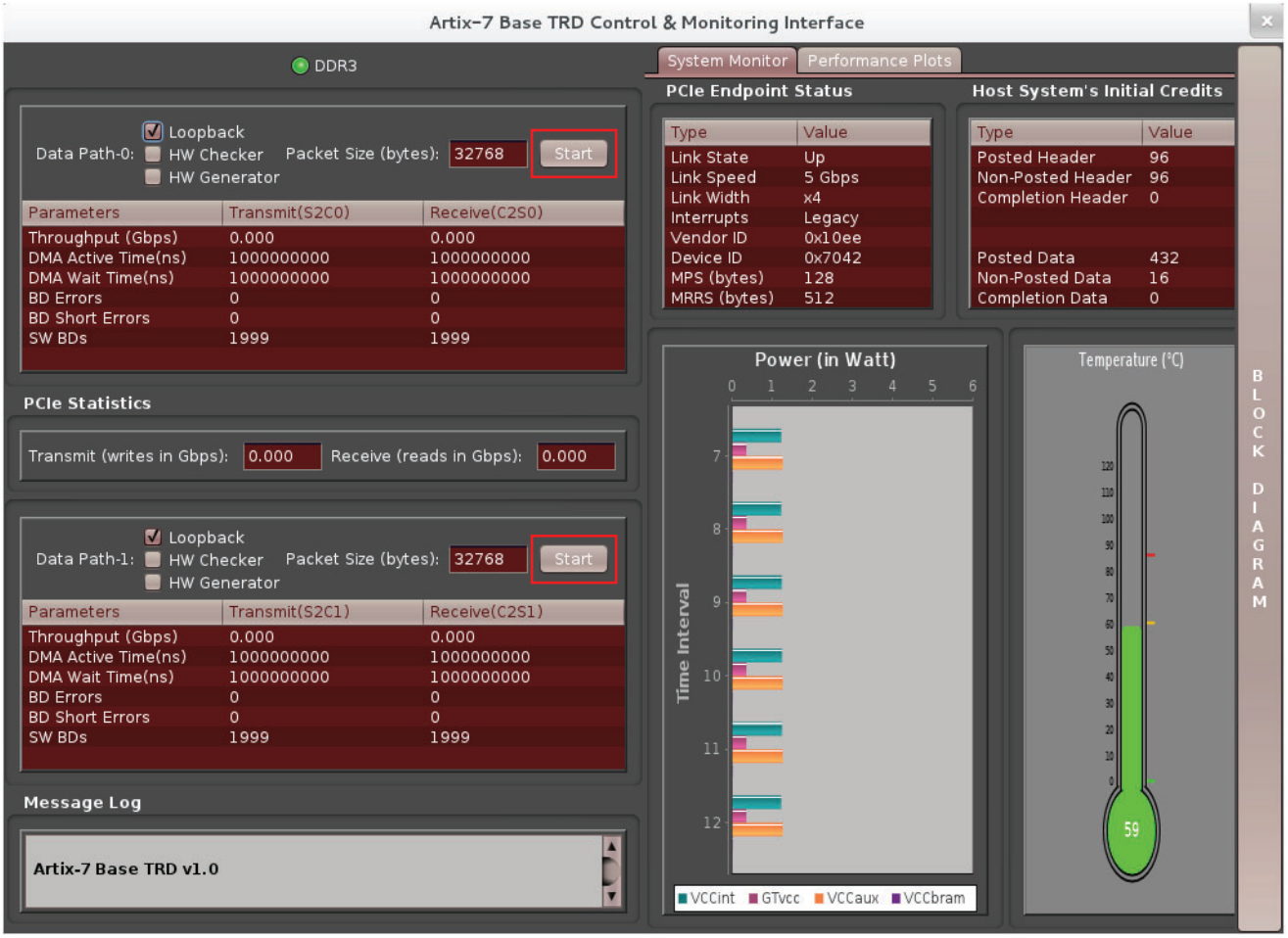


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Figure 26: **Start Data Traffic from GUI**

2. Verify TRD operations through the status information provided by the GUI as shown in Figure 27:
   a. Verify PCIe endpoint throughput.
   b. Verify the DMA Channel throughput for Datapath-0.
   c. Verify the DMA Channel throughput for Datapath-1.
   d. Verify that there are no buffer descriptor errors for error-free operation.

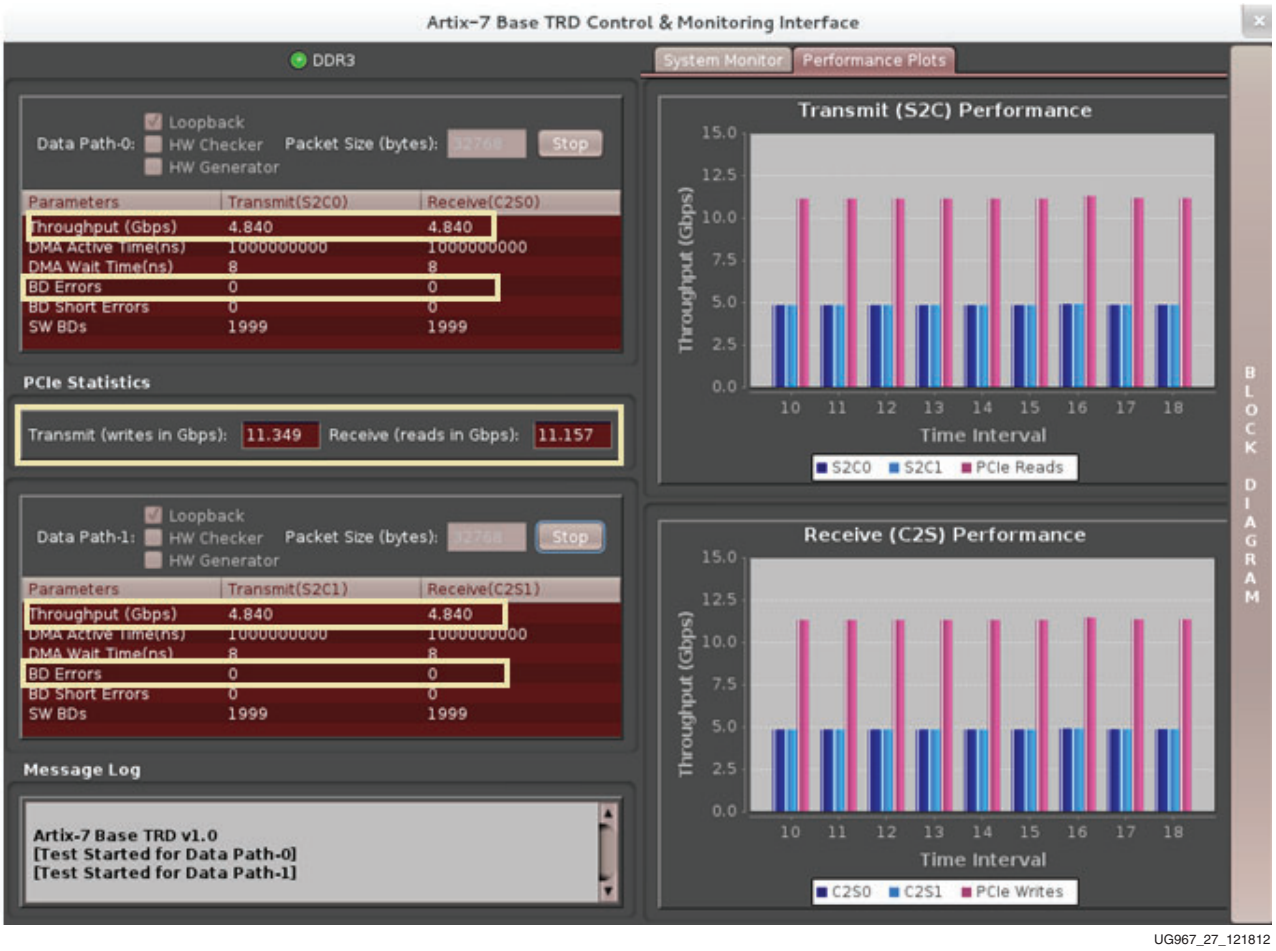

Figure 27: **Verifying Error-free Operation and Performance Plots**

3. Click the **Performance Plots** tab. The system-to-card and card-to-system performance numbers for a specific packet size are shown. The packet size can be adjusted and the resulting performance variation observed.
4. Close the GUI. This uninstalls the driver and opens the driver installation options screen of the Artix-7 FPGA base TRD. Driver un-installation requires the control and monitoring GUI to first be closed.

This completes system performance evaluation of the Artix-7 FPGA base TRD using the pre-built demonstration bit file. The reference design can now be modified. The Vivado Design Suite must be installed before proceeding with custom modifications. The design tools do not need to be installed on the same host PC in which the AC701 evaluation board is installed.

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Appendix A

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website.

For continual updates, add the Answer Record to your myAlerts.

For definitions and terms, see the Xilinx Glossary.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

The most up to date information related to the AC701 Evaluation Kit and its documentation is available on these websites:

AC701 Evaluation Kit

AC701 Evaluation Kit Documentation

AC701 Evaluation Kit Master Answer Record (AR 51900)

Artix-7 FPGA Base Targeted Reference Design Master Answer Record (AR 53372)

These Xilinx documents and sites provide supplemental material useful with this guide:

1. *AC701 Evaluation Board for the Artix-7 FPGA User Guide* (UG952)
2. *7 Series FPGA AMS Targeted Reference Design User Guide* (UG960)
3. *Vivado Design Suite User Guide Release Notes, Installation, and Licensing* (UG973)
4. *7 Series FPGAs Integrated Block for PCI Express User Guide* (PG054)
5. *Synthesis and Simulation Design Guide* (UG626)
6. *Vivado Design Suite Logic Simulation User Guide* (UG900)
7. *Understanding Performance of PCI Express Systems* (WP350)
8. *LogiCORE IP Aurora 8B/10B v7.1 User Guide* (UG766)
9. *LogiCORE IP Aurora 8B/10B v10.0 Product Guide for Vivado Design Suite* (PG046)
10. *LogiCORE IP AXI4-Stream Interconnect v1.1 Product Guide* (PG035)
11. *LogiCORE IP AXI Virtual FIFO Controller v1.1 Product Guide* (PG038)

12. *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476)
13. *7 Series FPGAs Memory Interface Solutions User Guide* (UG586)
14. *Artix-7 FPGA Integrated Block for PCI Express* (UG477)
15. *AC701 Evaluation Board for the Artix-7 FPGA User Guide* (UG952)
16. *AMS101 Evaluation Card User Guide* (UG886)

Additional References

These external websites provide supplemental material useful with this guide:

17. Northwest Logic
    (PCI Express® Solution, DMA Back End Core)
18. Fedora Project
    (Fedora operating system information and downloads)
19. PicoBlaze 8-bit Microcontroller
    (PicoBlaze™ 8-bit Microcontroller information and download)
20. Vivado Design Suite product page
    (Vivado® Design Suite information and downloads)
21. Artix-7 FPGA Product Table
    (List of Artix®-7 FPGAs)
22. Silicon Labs
    Si570, Si5324C, CP2103GM, VCP Drivers

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Appendix B

Warranty

THIS LIMITED WARRANTY applies solely to standard hardware development boards and standard hardware programming cables manufactured by or on behalf of Xilinx ("Development Systems"). Subject to the limitations herein, Xilinx warrants that Development Systems, when delivered by Xilinx or its authorized distributor, for ninety (90) days following the delivery date, will be free from defects in material and workmanship and will substantially conform to Xilinx publicly available specifications for such products in effect at the time of delivery. This limited warranty excludes:
(i) engineering samples or beta versions of Development Systems (which are provided "AS IS" without warranty); (ii) design defects or errors known as "errata";
(iii) Development Systems procured through unauthorized third parties; and
(iv) Development Systems that have been subject to misuse, mishandling, accident, alteration, neglect, unauthorized repair or installation. Furthermore, this limited warranty shall not apply to the use of covered products in an application or environment that is not within Xilinx specifications or in the event of any act, error, neglect or default of Customer. For any breach by Xilinx of this limited warranty, the exclusive remedy of Customer and the sole liability of Xilinx shall be, at the option of Xilinx, to replace or repair the affected products, or to refund to Customer the price of the affected products. The availability of replacement products is subject to product discontinuation policies at Xilinx. Customer may not return product without first obtaining a customer return material authorization (RMA) number from Xilinx.

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